In the Claims:

Please amend claims 1, 3, 10, 14, 15 and 30, and add new claims 31-32 as follows:

1. (Currently amended) A processor adapted to receive instructions in one of first and second external instruction formats F1 and F2, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each said external format F1 and F2 having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each said opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of external formats F1 and F2 being a common F1-F2 opcode bit in the format concerned so that each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$, the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to ~~translates~~translate each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

~~wherein~~wherein:

~~each said external format has one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears;~~

~~at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format;~~

each said first operation is specifiable in both said ~~first and second~~ external formats F1 and F2, and each said second operation is specifiable in said second external format F2;

all said first operations and all said second operations have distinct opcodes in said second external format F2; and

for every one of the first operations which the processor is capable of executing, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another~~the instruction specifying that operation in said first external format is identical, in each said common opcode bit, to the instruction specifying that operation in said second external format~~.

2. (Cancelled)

3. (Currently amended) A processor as claimed in claim 1, also adapted to receive instructions in a third external instruction format F3, said third external format F3 having one or more ~~preselected~~ opcode bits in which an opcode, specifying the operation to be executed, appears,

wherein:

each said opcode bit in one of said external formats F2 and F3 that has an individually corresponding opcode bit in the other one of the formats F2 and F3 is a common F2-F3 opcode bit in the format concerned so that each of said external formats F2 and F3 has, among its said one or more opcode bits, the same number C' of common F2-F3 opcode bits in total, where C' ≥ 1, ~~at least one said preselected opcode bit of said third external format being a further common opcode bit which is also one of said preselected opcode bits of said second external format;~~

~~wherein:~~

the or each said execution unit receives instructions in at least one of first and second internal instruction formats G1 and G2 and executes the operations specified thereby;

each said second operation is specifiable in both said second and third external formats F2 and F3;

said at least one instruction translation unit translates an instruction specifying said first operation in either said first or second external format F1 or F2 into said first internal format G1, and translates an instruction specifying said second operation in

either said second or third external format F2 or F3 into said second internal format G2; and

for every one of the second operations which the processor is capable of executing, all the mutually-corresponding common F2-F3 opcode bits in the two external formats F2 and F3 are identical to one another~~the instruction specifying that operation in said second external format is identical, in each said further common opcode bit, to the instruction specifying that operation in said third external format~~.

4. (Cancelled)

5. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

6. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

7. (Original) A processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel.

8. (Original) A processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats.

9. (Previously presented) A processor as claimed in claim 1, wherein said first external format has an instruction width different from that of said second external format.

10. (Previously presented) A processor as claimed in claim 1, wherein:

said at least one translation unit performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode.

11. (Original) A processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction.

12. (Original) A processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode.

13. (Original) A processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format.

14. (Currently amended) A machine-readable medium storing instructions to be executed by a processor,

the processor being adapted to receive instructions in one of first and second external instruction formats F1 and F2, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each said external format F1 and F2 having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each said opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of external formats F1 and F2 being a common F1-F2 opcode bit in the format concerned so that each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$,

and the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to

~~translates~~translate each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

~~wherein~~wherein:

~~each said external format has one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears;~~

~~at least one said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselcted opcode bits of said second external format;~~

each said first operation is specifiable in both said ~~first and second~~ external formats F1 and F2, and each said second operation is specifiable in said second external format F2;

all said first operations and all said second operations have distinct opcodes in said second external format F2; and

for every one of the first operations which the processor is capable of executing, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another ~~the instruction specifying that operation in said first external format is identical, in each said common opcode bit, to the instruction specifying that operation in said second external format~~.

15. (Currently amended) A method of encoding processor instructions for a processor, the processor being adapted to receive instructions in one of first and second external instruction formats F1 and F2, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each said external format F1 and F2 having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each said opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of external formats F1 and F2 being a common F1-F2 opcode bit in the format concerned so that each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$,

and the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to ~~translates~~translate each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

~~whereinwherein:~~

~~each said external format has one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears;~~

~~at least one said preselected opcode bit of said first external format is a~~

~~common opcode bit which is also one of said preselcted opcode bits of said second external format;~~

each said first operation is specifiable in both said ~~first and second~~ external formats F1 and F2, and each said second operation is specifiable in said second external format F2, said method comprising:

encoding all said first operations and all said second operations with distinct opcodes in said second external format F2;

encoding the opcodes of the first operations in said first and second external formats so that, for every one of the first operations which the processor is capable of executing, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another ~~the instruction specifying that operation in said first external format is identical, in each said common opcode bit, to the instruction specifying that operation in said second external format~~; and

storing the instructions having the encoded opcodes on a machine-readable medium.

16-29. (Cancelled)

30. (Currently amended) A propagated signal embodying instructions to be executed by a processor ~~the instructions comprising first and second external instruction formats, each instruction specifying one of a plurality of first operations executable by the~~

~~processor or one of a plurality of second operations executable by the processor~~, the processor being adapted to receive instructions in one of first and second external instruction formats F1 and F2, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor and each said external format F1 and F2 having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each said opcode bit in one of external formats F1 and F2 that has an individually corresponding opcode bit in the other one of external formats F1 and F2 being a common F1-F2 opcode bit in the format concerned so that each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$, and the ~~wherein the instructions, when executed by a~~] processor comprising:[~~, cause the processor to perform the steps of~~

at least one execution unit which receives ~~receiving~~ the instructions in an internal instruction format and executes ~~executing~~ the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to translate ~~translating~~ each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

~~whereinwherein:~~ ~~each said external format has one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears;~~

~~at least one said preselected opcode bit of said first external format is a~~

~~common opcode bit which is also one of said preselected opcode bits of said second external format;~~

each said first operation is specifiable in both said ~~first and second~~ external formats F1 and F2, and each said second operation is specifiable in said second external format F2;

all said first operations and all said second operations have distinct opcodes in said second external format F2; and

for every one of the first operations which the processor is capable of executing, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another ~~the instruction specifying that operation in said first external format is identical, in each said common opcode bit, to the instruction specifying that operation in said second external format~~.

31. (New) A processor as claimed in claim 1, wherein the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 both have the same bit position.

32. (New) A processor adapted to receive instructions in one of first and second external instruction formats, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each said external format having one or more opcode bits in which an

opcode, specifying the operation to be executed, appears, and each bit position at which the first and second external formats both have respective opcode bits is a common bit position;

the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to translate each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

wherein:

each said first operation is specifiable in both said first and second external formats, and each said second operation is specifiable in said second external format;

all said first operations and all second operations have distinct opcodes in said second external format; and

for every one of the first operations which the processor is capable of executing, the first and second external formats have identical opcode bits in each said common bit position.